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New and emerging applications in the consumer and mobile space, the growing impact of the Internet of Things (IoT) and wearable electronics (WE), and the slowdown of Moore's law have been driving many new trends and innovations in advanced packaging technology. The semiconductor industry now has to focus on integration and system scaling to meet the ever-increasing electronic system demands for performance and functionality as well as the reduction of form factor, power consumption and cost. This paradigm shift from chip-scaling to system-scaling will re-invent microelectronics packaging, continue driving system bandwidth and performance, and help sustain Moore's Law. It also drives overall demand for maximum functional integration in the smallest and thinnest package with the lowest cost. The challenge for the semiconductor industry is to develop a disruptive packaging technology platform capable of achieving these goals. The most promising solutions in volume production today are advanced Wafer Level Packaging, such as Fan-out Wafer Level Packaging (FOWLP), embedded Wafer Level Ball Grid Array (eWLB) which provides significant bandwidth, performance, form factor and cost benefits compared to other packaging technologies available today.

This article will discuss the wide range of FOWLP/eWLB adoptions and new features available for mobile, IoT and WE. This advanced technology is well designed for RF, MEMS/sensors, 3D SiP modules as well as thin, highly integrated packaging solutions. Innovative FOWLP/eWLB features will be also introduced with the merits and characterization data for specific applications.

The emergence and evolution of any package technology is driven by market trends as experienced by the end application. With the maturing of the mobile market, the trends for smartphones and other mobile devices are more than ever for lower cost. Meanwhile, a higher degree of functionality and performance, thinner devices, and longer battery life are some of the additional market drivers seen in these devices. The implications of these market drivers on the

### *Next-generation Packaging Requirements*

Semiconductor packaging has a significant impact on the overall device performance. Traditional packaging technologies are reaching their limits in terms of the performance, size and scalability required to meet the needs of emerging applications. Current and future demands of microelectronic systems in terms of performance, power consumption and reliability at a required cost are met by developing advanced silicon process technology, innovative packaging solutions based on chip and package system co-design, low cost materials, reliable interconnect technologies, and advanced assembly and test.

For internet connected devices, there are four interrelated requirements for an effective packaging solution: 1) Cost effectiveness, 2) Thinner and smaller form factor, 3) High performance, and 4) Integration. For mobile, IoT and WE devices, three types of integrated circuits (ICs) will be the primary drivers of semiconductor growth: 1) Specialized low-power microcontrollers (MCUs, embedded processors with non-volatile memory (NVM) and power management functions); 2) Connectivity (Wi-Fi, Bluetooth®, GPS, cellular, ZigBee®, etc.); 3) Sensors and actuators (MEMS, image sensors, others).

These applications listed above and ICs require different process technology nodes and different process technologies—MCU (digital + mixed-signal + non-volatile memory), connectivity (RF + analog + antenna/security) and sensors (MEMS and non-MEMS). System-on-chip (SoC) could be an attractive solution if different functions can be placed in the same wafer fab solution. However, achieving such an all-in-one SoC solution can be quite difficult and often very costly. An alternative approach is to balance silicon-level and package-level integration, as evidenced by rapid expansion of system-in-package (SiP) modules. SiP modules provide the ability to not only integrate multiple technologies, but also additional components such as passives, antennas, etc., to create fully functional sub-systems. To illustrate the potential for miniaturization by use of SiP modules, Xiaomi's low-cost, high- performance MI3 smartphone, for example, contained approximately 850 electronic components, including ~22 filters, ceramic crystals, oscillators, ~103 diodes and small transistors, and ~670 passives.

### *Advanced Wafer-Level Technology ; eWLB/FO-WLP*

As a small, lightweight, high performance semiconductor package, wafer-level chip-scale packaging (WLCSP) has been a popular solution for space constrained mobile devices and is a compelling solution for new IoT and WE applications. WLCSP was introduced in the late 1990s as a semiconductor package wherein all manufacturing operations are performed in wafer form with dielectrics, thin-film metals and solder bumps applied directly on the surface of the die with no additional packaging [2]. The WLCSP provides the smallest possible package size since—the final package is no larger than the die itself. The volume of WLCSP used in the industry has experienced steady growth – driven by the small form factor and high-performance requirements of mobile consumer products.

For emerging applications requiring significantly higher performance and bandwidth, a transition from fan-in WLCSP to fan-out wafer-level packaging (FOWLP) is often required to achieve maximum connection density, improved electrical and thermal performance and small package dimensions. FOWLP, also known as embedded wafer-level ball grid array (eWLB), is a versatile interconnection system processed directly on the wafer and is compatible with motherboard technology pitch requirements. Unlike fan-in wafer-level packaging, eWLB is not constrained by the semiconductor die size.

eWLB technology addresses a wide range of factors for mobile, IoT and WE applications. At one end of the spectrum is the need for a significant increase in input/output (I/O) density, a particular challenge as packages become progressively smaller and thinner. eWLB achieves fine line width and spacing as well as superior electrical performance, providing more design flexibility and a significant reduction in size than is possible with printed circuit board (PCB) technology. eWLB also provides the ability to integrate different active and passive elements, embedded very close to each other as an SiP. Complex thermal issues related to power consumption and device's electrical performance (including electrical parasitic and operating frequency) are successfully addressed by eWLB technology [3].

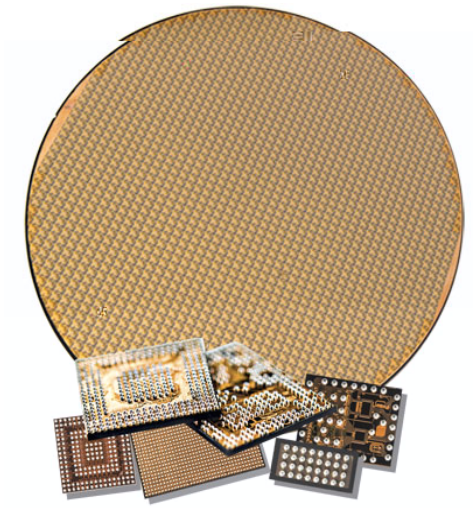
On the other side of the spectrum is the need to reduce assembly and test costs to meet consumer requirements for mobile, IoT and WE. The manufacturing process for eWLB is well established and lends itself to the use of large wafer and panel sizes, which provides compelling cost reductions over conventional wafer-level processing. The advantages of the unique manufacturing process are covered later in this article.

### *eWLB/FO-WLP for Mobile, IoT and WE Applications*

As demonstrated by the evolution of cellular phones, product differentiation today is driven by ever-expanding functionality, feature sets, and faster communications. At the same time, consumers have made clear their desires for feature-rich products in compact form factors for portability. eWLB provides the smallest possible yet highest performing semiconductors. Currently all leading mobile products as well as some consumer electronics contain eWLB packages that are baseband processors, RF transceivers, connectivity devices, near field communication (NFC), security devices, MCUs, memory, memory controllers, RF MEMS and power management ICs (PMICs). There have been new opportunities and accelerated customer adoption in areas such as logic processors, MEMS, audio devices, fingerprint sensors and automotive devices.

In a number of cases, eWLB achieved a 20~40% reduction in package size as compared to other packaging solutions and over 50% volume reduction because of its slim and smaller form factor. For RF and high-frequency devices, eWLB showed less parasitic electrical performance, thus therefore, it also significantly improved overall device performance. In one example, a 77GHz SiGe mixer packaged as an eWLB achieved excellent high- frequency electrical performance due to because of the small contact dimensions and short signal pathways which that decreased parasitic effects. Higher power efficiency was found in eWLB solutions for PMIC devices compared to other package solutions. In terms of advanced

silicon (Si) nodes, eWLB solutions are in high-volume production on 28nm and starting to ramp on 20nm devices.



eWLB products found in various mobile products and consumer electronics

There are a number of cases where eWLB has helped semiconductor companies achieve very specific and measureable results. Following are some examples as shown in Figure 3:

Redistribution layers (RDL) in eWLB are utilized for higher electrical performance and complex routing to meet electrical requirements (Figure 3a). RDL also can provide embedded passives (R, L, C) using a multi-layer structure. Excellent performance of transmission lines was reported in manufacturing eWLB (insertion loss 0.1dB/mm @ 10GHz, 0.25dB/mm @ 60GHz). Inductors in eWLB offer significantly better performance compared to inductors in standard on-chip technologies. Further improvement of the quality factor of the integrated inductor and capacitors by using low-loss thin-film dielectrics and molding compound in eWLB was reported as well.

FOWLP in a 3D configuration has received considerable customer interest for memory and advanced application processors by virtue of the higher routing density and form factor reduction. The requirement for SiP integration is also a growing trend for advanced application processors, MEMS and sensors in wearable electronics as way to cost-effectively achieve advanced silicon die partitioning for increased performance and integration in a reduced form factor. Figure 3b shows one of example of SiP eWLB which that has a number of discretes in the top package and is pre-stacked on the bottom eWLB to form a 3D SiP module with a thin profile. One example of the end application or device benefiting from such a 3D packaging concept could be an RF-FEM where the CMOS die is located in the bottom eWLB package, and other components including SAW filters, passives, duplexer, and low-noise amplifier (LNA) located in the top FBGA package. Discretes are removed from the motherboard and relocated in the top package for a reduction in the space required on the mother board. Discretes are also more effective when they are close to the device, which significantly improves the overall performance as well as provides a power saving advantage. This SiP eWLB has demonstrated more attractive power efficiency performance compared to conventional packaging and it is representative of a significantly smaller packaging solution that is well-suited for IoT or WE devices.

Side-by-side multi-chip packaging can provide more design flexibility for SiP applications because a chip designer has more freedom in pad location, as well as circuit block allocation, as shown in Figure 3c. The 2.5D eWLB technology utilizes very fine-pitch metal line width and spacing as well as multi-layer RDL processing, providing better technical solutions for multi-chip packaging. Multi-die eWLB has already been in high-volume manufacturing for the last three years in applications such as RF, SoC, PMIC, and memory devices. Discrete multi-layer ceramic chip (MLCC) capacitors and integrated passive embedding have also been successfully demonstrated and qualified.

To enable higher interconnection density and signal routing, packages with multi-layer RDL and fine line/width spacing are fabricated and implemented on the eWLB platform. There are a number of development activities focused on further enhancements to highly integrated eWLB packaging solutions including finer line/space widths down to 2/2µm, ultra-thin package profiles (currently qualified for 0.3mm including solder ball) and multi-layer RLD (above 3 layers)[4]. Innovative structure optimization of 2.5D/3D eWLB provides dual advantages of both height reduction and enhanced package reliability.

Value Propositions of 3D eWLB-PoP

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Successful reliability and mechanical/thermal characterization results on 3D eWLB-PoP package configurations demonstrate the capabilities of eWLB as an enabling technology for highly integrated miniaturized, low profile, and cost-effective solutions [5]. 3D eWLB-PoP is designed to meet the lower profile PoP requirement for mobile or tablet application with cost-effective solution. 3D eWLB-

PoP bottom has 300um package height so total stacked PoP height could be less than 0.8 mm after top memory package stacking (body thickness of 0.45mm). Table 1 shows value proposition of 3D eWLB-PoP technology.

(a) (b)

(c) (d)

(e)

WLPs, such as low assembly cost, minimum dimensions and height, as well as excellent electrical and thermal performance, are equally true for eWLB. The differentiating factors with eWLB are the ability to integrate passives like inductors, resistors and capacitors into the various thin-film layers, active/passive devices into the mold compound, and achieve 3D vertical interconnections for new SiP and 2.5D/3D packaging solutions. 3D eWLB-PoP / SiP eWLB-PoP technology provides more value-add in performance and promises to be a new packaging platform that can expand its application range to various types of mobile/portable devices as well as 3D SiP systems.


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